Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (original): An apparatus for indicating the insertion and removal of a circuit board for hot swap applications comprising:

a logic circuit having at least one input and at least one output; and

a time extender circuit connected to said logic circuit, for extending an output signal of said logic circuit for a period of time after said circuit board is completely inserted and removed.

Claim 2 (original): The apparatus according to claim 1, wherein said logic circuit further comprises a NAND gate.

Claim 3 (original): The apparatus according to claim 2, wherein said NAND gate further comprises:

a plurality of transistors connected in parallel having a plurality of inputs and at least one output.

Claim 4 (original): The apparatus according to claim 1, further comprising an enable logic gate connected to said at least one output of said logic circuit.

Claim 5 (original): The apparatus according to claim 1, further comprising a transistor configured as an open collector having an input and an output whose input is connected to said at least one output of said logic circuit.

Claim 6 (original): The apparatus according to claim 1, wherein said time extender circuit further comprises:

a resistor connected between ground and said logic circuit; and

a capacitor connected between a voltage and said logic circuit.

Claim 7 (original): The apparatus according to claim 2, further comprising at least one inverter having an input and an output, wherein said input of said at least one inverter is connected to an output of said NAND gate.

Claim 8 (original): The apparatus according to claim 3, further comprising at least one inverter having an input and an output, wherein said input of said at least one inverter is connected to said at least one output of said plurality of transistors.

Claim 9 (original): The apparatus according to claim 7, wherein said at least one inverter is a Schmitt trigger inverter.

Claim 10 (original): The apparatus according to claim 8, wherein said at least one inverter is a Schmitt trigger inverter.

Claim 11 (original): The apparatus according to claim 8, further comprising:

an enable logic gate connected to at least one of said outputs of said at least one inverter; and

a transistor configured as an open collector having an input and an output whose input is connected to at least one of said outputs of said at least one inverter.

Claim 12 (original): An apparatus for indicating the insertion and removal of a circuit board, comprising:

a plurality of transistors connected in parallel having at least two inputs and at least one output;

at least one other transistor having at least one output and at least one input connected to said at least one output of said plurality of transistors connected in parallel;

at least one Schmitt trigger inverter having an input connected to said output of said at least one other transistor; and

a time extender circuit connected to said at least one output of said at least one other transistor.

Claim 13 (original): The apparatus according to claim 12, further comprising a transistor configured as an open collector having an input and an output whose input is connected to said output of said at least one Schmitt trigger inverter.

Claim 14 (original): A method for indicating the insertion and removal of a circuit board, comprising:

receiving at least one input signal indicating the insertion and removal of a circuit board;

processing said at least one input signal indicating the insertion and removal of a circuit board;

generating an output signal indicating said insertion and said removal of said circuit board; and

extending said output signal for a period of time after said circuit board is completely inserted and removed.

Claim 15 (original): The method according to claim 14, further comprising the step of enabling said output signal.

Claim 16 (original): The method according to claim 14, further comprising the step of inverting said output signal.

Claim 17 (original): The method according to claim 14, wherein said step of extending said output signal for a period of time after said circuit board is completely inserted or extracted further comprises the step of discharging a capacitor.

Claim 18 (original): The method according to claim 14, further comprising the steps of:

outputting a plurality of complementary control signals;

performing a logic operation using one of said complementary control signals and said output signal to produce a logic output;

using said logic output from said logic operation to source current; and

sinking current using said output signal.

Claim 19 (original): The method according to claim 17, wherein said step of processing further comprises the step of performing a logic function on said at least one input signal.

Claim 20 (original): The method according to claim 19, wherein said logic function further comprises the step of performing a NAND logic function on said at least one input signal.

Claim 21 (original): A method for outputting single ended or differential signals, comprising:

outputting a plurality of complementary control signals;

performing a logic operation using one of said complementary control signals and an input signal to produce an output;

using said output from said logic operation to source current;

sinking current using said input signal.

Claim 22 (original): The method of claim 21, wherein said step of sinking current further comprises using another of said plurality of complementary control signals to sink said current to ground or through a resistor to ground.

Claim 23 (original): The method of claim 21, wherein said step of outputting a plurality of complementary control signals further comprises applying a threshold voltage.